Amendments to the Claims:

Please replace all prior versions, and listings of claims in the application with the following listing of claims.

Listing of claims

Claim 1 (currently amended): A data processing architecture comprising:

an input device for receiving an incoming stream of data packets of unpredictable size; and

a plurality of processing elements which are operable to process data received thereby and to store different amounts of data;

wherein the input device is operable to distribute batches of data packets of unpredictable size ~~in batches~~ across said processing elements such that the number of said processing elements across which each data packet is distributed is dynamically determined based at least in part on the size of the data packet;

a data packet greater than a predetermined size being divided into portions and each portion distributed to a respective processing element; and

a data packet less than a predetermined size being distributed to a single processing element;

wherein the data processing architecture is operable to process at least one data packet at a time.

Claim 2 (original): A data processing architecture as claimed in claim 1, wherein the processing elements are arranged in a single instruction multiple data (SIMD) array.

Claim 3 (previously presented): A data processing architecture as claimed in claim 1, wherein a data packet is allocated to as many processing elements as are necessary to store said packet and to process said packet.

Claim 4 (previously presented): A data processing architecture as claimed in claim 1, wherein the portions are of a fixed size.

Claim 5 (canceled)

Claim 6 (original): A data processing architecture as claimed in claim 1, wherein the input device is operable to transfer data packets to the processing elements such that not all processing elements receive data.

Claim 7 (previously presented): A data processing architecture as claimed in claim 1, wherein the processing elements are operable to control the transfer of packet portions to the processing elements from the input device.

Claim 8 (original): A data processing architecture as claimed in claim 7, wherein the processing elements are operable to control the input device by means of software.

Claim 9 (previously presented): A data processing architecture as claimed in claim 1, wherein the processing elements are operable to control the transfer of packet portions from the processing elements to an output device.

Claim 10 (canceled)

Claim 11 (currently amended): A data processing architecture as claimed in claim 9, wherein a plurality of said input ~~devices~~ device and said output ~~devices~~ device form part of a plurality of input/output systems, operable to transmit data to, and receive data from, the processing elements and adapted to support multiple input/output operations.

Claim 12 (previously presented): A data processing architecture as claimed in claim 1, comprising a single instruction multiple data (SIMD) data processing architecture,

wherein at least one processing element is operable to enter a standby mode of operation in dependence upon data received by that processing element.

Claim 13 (previously presented): A data processing architecture as claimed in claim 12, wherein the at least one processing element is operable to enter the standby mode of operation when no data is received.

Claims 14 and 15 (canceled)

Claim 16 (previously presented): A data processing architecture as claimed in claim 1, comprising a first plurality of parallel arrays of processing elements, and a second plurality of hardware accelerator units.

Claim 17 (previously presented): A data processing architecture as claimed in claim 1, comprising a plurality of parallel arrays of said processing elements, and a data input/output system which is operable to transfer data to and from the arrays of processing elements in turn.

Claim 18 (canceled)

Claim 19 (previously presented): A data processing architecture as claimed in claim 2, wherein each processing element is operable to process data stored by that element in accordance with processing steps determined by the data concerned.

Claim 20 (previously presented): A data processing architecture as claimed in claim 1, comprising a plurality of functional blocks chosen from: a single instruction multiple data (SIMD) processing element array, a data input device, a data output device, a hardware accelerator, a data packet buffer and a bus structure for connecting the functional blocks to one another.

Claim 21 (previously presented): A data processing architecture as claimed in claim 1, implemented on a single integrated circuit.

Claim 22 (previously presented): A data processing architecture as claimed in claim 1, implemented on a plurality of integrated circuits.

Claims 23-31 (canceled)

Claim 32 (previously presented): A processor comprising a data processing architecture as claimed in claim 1.

Claim 33 (canceled)

Claim 34 (previously presented): A data processing architecture as claimed in claim 1, wherein each processing element is operable to process data stored by that element in accordance with processing steps determined by the data concerned.

Claim 35 (original): A data processing architecture as claimed in claim 12, wherein each processing element is operable to process data stored by that element in accordance with processing steps determined by the data concerned.

Claims 36 and 37 (canceled)

Claim 38 (original): A data processing architecture as claimed in claim 17, wherein each processing element is operable to process data stored by that element in accordance with processing steps determined by the data concerned.

Claim 39 (canceled)

Claim 40 (previously presented): A data processing architecture as claimed in claim 1, implemented on a single integrated circuit.

Claim 41 (original): A data processing architecture as claimed in claim 12, implemented on a single integrated circuit.

Claims 42 and 43 (canceled)

Claim 44 (original): A data processing architecture as claimed in claim 17, implemented on a single integrated circuit.

Claims 45 and 46 (canceled)

Claim 47 (previously presented): A data processing architecture as claimed in claim 12, implemented on a plurality of integrated circuits.

Claims 48 and 49 (canceled)

Claim 50 (currently amended): A data processing architecture as claimed in claim 17, implemented on a plurality of integrated circuits.

Claim 51 (canceled)

Claim 52 (previously presented): A processor comprising a data processing architecture as claimed in claim 1.

Claim 53 (previously presented): A processor comprising a data processing architecture as claimed in claim 12.

Claims 54 and 55 (canceled)

Claim 56 (previously presented): A processor comprising a data processing architecture as claimed in claim 17.

Claims 57 and 58 (canceled)

Claim 59 (previously presented): A data processing architecture as claimed in claim 9, wherein said output device is operable to collect processor data packets from the processing elements and to construct an outgoing data packet stream from collected processor data packets.

Claim 60 (previously presented): A data processing architecture as claimed in claim 9, wherein said input device and said output device are part of an input/output system operable to transmit data to, and receive data from, the processing elements.

Claim 61 (previously presented): A data processing architecture as claimed in claim 1, wherein processing is only performed by processing elements containing packets or packet portions carrying a header.

Claim 62 (previously presented): A data processing architecture as claimed in claim 1, wherein processing is performed by multiple processing elements containing portions of a packet, in dependence on either data in the packet or information about the packet.

Claim 63 (previously presented): A data processing architecture as claimed in claim 1, wherein the number of processing elements is determined based on a bandwidth and an amount of required processing.

Claim 64 (previously presented): A data processing architecture as claimed in claim 1, wherein the size of the packet portions is determined based on a bandwidth and an amount of required processing.